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| APPLICATION NO.   | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO.         | CONFIRMATION NO. |
|---|-------------|----------------------|-----------------------------|------------------|
| 10/012,207  | 11/05/2001  | Vibha Goel           | 11971-012001/               | 5310             |
| 20985   | 7590        | 03/29/2005           |                             |                  |
| FISH & RICHARDSON, PC<br>12390 EL CAMINO REAL<br>SAN DIEGO, CA 92130-2081 |             |                      | EXAMINER<br>SEDIGHIAN, REZA |                  |
|   |             |                      | ART UNIT                    | PAPER NUMBER     |
|   |             |                      | 2633                        |                  |
| DATE MAILED: 03/29/2005   |             |                      |                             |                  |

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/012,207

Applicant(s)

GOEL, VIBHA

Examiner

M. R. Sedighian

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 05 November 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-31 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-31 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 05 November 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 5/9/02.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

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1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 30 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As to claim 30, it is not clear what is meant by "... wherein said compensating comprises forming a switching path which sends signals to routers which do not signal errors therein".

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-22 and 31 are rejected under 35 U.S.C. 102(b) as being anticipated by Shiragaki (US Patent No: 5,663,820).

Regarding claim 1, Shiragaki teaches a signal switching system (fig. 4), comprising: a signal switching part (40, fig. 4) receiving a plurality of inputs and switching any of the plurality of inputs to any of a plurality of outputs (col. 5, lines 17-23); an optical router (the optical routing and switching system of node B, fig. 4) receiving the signals from the outputs and optically routing (50, 54, 56, 59, fig. 4) the signals (col. 5, lines 30-40), wherein the optical router (50, 54, 56, 59 of node B in fig. 4) including a fault detection element (53, fig. 4) which produces a fault signal to the

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switching part (col. 5, lines 41-55), and wherein the switching part (40, fig. 4) responding to the fault signal to switch one of the inputs to one of the outputs based on the fault signal (col. 5, lines 52-55).

Regarding claim 2, Shiragaki teaches the switch part includes an  $n$  by  $n$  switch (switch 40 is a  $n \times n$  switch), wherein at least a plurality of the channels are redundancy channels (some of the input channels to the switch 40 can be redundant channels).

Regarding claim 3, Shiragaki teaches the switching part includes an optical switch (40, fig. 4).

Regarding claims 4-5, Shiragaki teaches the switching part includes a  $16 \times 16$  switch, or  $8 \times 8$  switch (note that switch 40 has  $n$  inputs and  $n$  outputs, for example it can be an  $8 \times 8$  switch, or a  $16 \times 16$  switch).

Regarding claim 6, Shiragaki teaches the optical switch includes an optical detecting element which detects a signal on one of the optical lines (col. 5, lines 50-52).

Regarding claim 7, Shiragaki teaches the signal is formed as an amplitude modulated signal on the optical lines (col. 7, lines 15-35).

Regarding claim 8, Shiragaki teaches sending a plurality of channels to a plurality of routers (col. 5, lines 30-35 and 50, fig. 4, note that optical signals propagating on fibers 47 are demultiplexed, or routed by respective demultiplexers 50), wherein the routers have a spare capability for failed routers (col. 5, lines 41-55, note that if one of the transmission line 47 fails, another one of the transmission line 47 can be selected, and another demultiplexer 50 can be used to further route the signal); and providing an optical signal from the routers indicating failure in the routers (col. 5, lines 41-55).

Regarding claims 9-10, Shiragaki teaches the signal is formed as an amplitude modulated signal on the optical lines (col. 7, lines 15-35)..

Regarding claim 11, Shiragaki teaches sampling an optical signal as part of sending to determine the failure signal (col. 5, lines 35-40).

Regarding claim 12, Shiragaki teaches the signal is formed as an amplitude modulated signal on the optical lines (col. 7, lines 15-35).

Regarding claim 13, Shiragaki teaches the signal include information indicative of a frequency of the error (col. 5, lines 41-48).

Regarding claim 14, Shiragaki teaches an all optical switch (40, fig. 4) capable of switching a plurality of inputs to outputs (switch 40 has many inputs and outputs) and having a control mechanism (41, fig. 4), and a router array (47, 50, fig. 4) producing an optical error signal indicative of errors in the router array (col. 5, lines 41-55), wherein the error signal being coupled (57, fig. 4) to the optical switch (40, fig. 4) and being used by the control mechanism (41, fig. 4 and 52-55).

Regarding claim 15, Shiragaki teaches the optical error signal is modulated on one of the outputs (col. 5, lines 43-45 and 51, 52, 55, 56, fig. 4).

Regarding claim 16, Shiragaki teaches the optical error signal is amplitude modulated on one of the elements (col. 5, lines 41-48).

Regarding claim 17, Shiragaki teaches an optical sampling element (51, fig. 4) which produces a sample (the output signal of combiner 51) indicative of the optical error signal.

Regarding claim 18, Shiragaki teaches the control mechanism operates based on electrical signals (col. 5, lines 36-37).

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Regarding claim 19, Shiragaki teaches the sampling element includes an optical to electrical converter (52, fig. 4) and a framer element (53, fig. 4) for producing an electrical signal which is used by the control mechanism (col. 5, lines 56-60).

Regarding claims 20-22, Shiragaki teaches the switching part is an nxn switch, or a 16x16 switch, or 8x8 switch (note that switch 40 has n inputs and n outputs, for example it can be an 8x8 switch, or a 16x16 switch).

Regarding claim 31, Shiragaki teaches an optical detecting device (46, fig. 4) which detects a control signal (the control signal generated by the controller 53) which is modulated (55, fig. 4) on one of the signals being switched (the control signal outputted by the E/O converter 55, added to the output of the switched signal out of switch 54).

5. Claims 23-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Holender (US Patent No: 5,729,548).

Regarding claim 23, Holender teaches a method comprising: carrying out all optical switching (810, fig. 8) between a plurality of channels (col. 9, lines 33-55) and a plurality of routers (805, 815, fig. 8).

Regarding claim 24, Holender teaches providing signaling from the plurality of routers (805, 815, fig. 8) to effect the optical switching (810, fig. 8).

Regarding claim 25, Holender teaches the signaling comprises determining errors in the routers and producing signals indicative of the errors (col. 10, lines 61-64, col. 11, lines 6-9, note that the connections through routers 805 and 815 are established by the controller 820 and are dynamically variable as to handle a failure).

Regarding claim 26, Holender teaches the signaling comprises inducing a signal indicative of the error on one of the optical channels (col. 10, lines 26-34).

Regarding claim 27, Holender teaches the inducing comprises amplitude modulating the signal on the optical channel (col. 2, lines 25-35, 43-52).

Regarding claim 28, Holender teaches the inducing comprises adding an indication of a channel number to the signal indicative of the error (col. 5, lines 11-13, 64-67, col. 6, lines 1-8).

Regarding claim 29, Holender teaches the switching comprises compensating for errors in the routers (col. 11, lines 6-9).


Regarding claim 30, as it is understood in view of the above 112 problem, Holender teaches the compensating comprises forming a switching path which sends signals to routers which do not have signal errors therein (col. 10, lines 29-34, col. 11, lines 4-9, note that controller 820 bidirectionally communicate and control each of the router 805 and 815 and the switch 810, and the connections through routers 805 and 815 are dynamically variable as to handle a failure).

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to M. R. Sedighian whose telephone number is (571) 272-3034. The examiner can normally be reached on M-F (from 9 AM to 5 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan can be reached on (571) 272-3022. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
**M. R. SEDIGHIAN**  
**PRIMARY EXAMINER**